



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/038,753	01/04/2002	Romeo Letor	854063.672	6284

500 7590 03/27/2003

SEED INTELLECTUAL PROPERTY LAW GROUP PLLC
701 FIFTH AVE
SUITE 6300
SEATTLE, WA 98104-7092

EXAMINER

DICKEY, THOMAS L

ART UNIT PAPER NUMBER

2826

DATE MAILED: 03/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/038,753

Applicant(s)

LETOR ET AL

Examiner

Thomas L Dickey

Art Unit

2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 May 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 15-17 and 19 is/are allowed.
- 6) ☒ Claim(s) 1-14 and 18 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 January 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☒ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

Art Unit: 2826

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 06 May 2002 is acceptable.

Drawings

2. The formal drawings filed on 04 January 2002 are acceptable.

Priority

3. Acknowledgment is made of applicant's claim for foreign priority based on an application filed at the European Patent Office on 01 January 2001. It is noted, however, that applicant has not filed a certified copy of the European Patent Office application as required by 35 U.S.C. 119(b).

Information Disclosure Statement

4. The Information Disclosure Statement filed on 04 January 2002 has been considered.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

Art Unit: 2826

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claims 1-14 and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, line 7, "said second high voltage region" has no antecedent basis. For examination purposes it is assumed that in line 8, applicant intends "a high voltage region" to read, "a second high voltage region," and that applicant intends the recital contained in line 8 to precede the recitation of "said second high voltage region."

In claim 7, line 2, "said high voltage region" has no antecedent basis. For examination purposes it is assumed that "said high voltage region" of line 2 refers to the element introduced as "a first high voltage region" in line 2 of claim 1.

In claim 7, line 3, "said high voltage region" has no antecedent basis. For examination purposes it is assumed that "said high voltage region" of line 3 refers to the element introduced as "a first high voltage region" in line 2 of claim 1.

In claim 14, line 3, "the high voltage region" has no antecedent basis. For examination purposes it is assumed that "the high voltage region" of line 3 refers to the element introduced as "a first high voltage region" in line 2.

In claim 18, line 3, "the high voltage region" has no antecedent basis. For examination purposes it is assumed that "the high voltage region" of line 3 refers to the element introduced as "a first high voltage region" in line 2.

Correction is required.

Art Unit: 2826

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1,6-9, and 13 rejected under 35 U.S.C. 102(a) as being anticipated by THE ADMITTED PRIOR ART.

The admitted prior art discloses a A n integrated power device comprising: a power component 60 (2 in figure 1) including a first high-voltage region 6 (referred to as the "collector region" as figure 1 is described), a low-voltage region 10 (referred to as the "emitter region" as figure 1 is described), a first unidirectional element (first diode) 25 and a second unidirectional element (second diode) 26 connected together between the first high-voltage region 6 and the low-voltage region 10, the first (first diode) 25 and the second (second diode) 26 unidirectional elements defining a common intermediate node 24, biasing means (shown schematically in figure 1 as part 3e) connected between the common intermediate node 24 and the second high-voltage region 30, and a control circuit 61 including the second high-voltage region 30, wherein the first (first diode) 25 and the second (second diode) 26 unidirectional elements are connected together in antiseriess (note the schematic inset on the right hand side of figure 2) through the common intermediate node 24, the first diode 25 has an anode region formed by the first high-voltage region 6, and a cathode region formed by a first epitaxial

Art Unit: 2826

layer 7 set on top of the first high-voltage region 6, the second diode 26 has a cathode region formed by a second epitaxial layer 8 set on top of the first epitaxial layer 7, and an anode region formed by a body region of the power component 60, the body region housed in the second epitaxial layer 8 beneath the low-voltage region 10, wherein the power component 60 is formed in a first chip, and the control circuit 61 is formed in a second chip, and wherein the power component 60 is an IGBT transistor, the high-voltage region is a collector region, and the low-voltage region 10 is an emitter-contact region. Note figures 1 and 2 and pages 1-5 of the instant application. Note that European Patent Application No. 0830051.9, referred to in the instant application, was published as EP-1120565A1 on 8 January 2001. In the first instance, this prior application does not disclose the admitted prior art as that application's invention, and in the second instance, that application was not made by the present applicants.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 10 and 11 rejected under 35 U.S.C. 103(a) as being unpatentable over THE ADMITTED PRIOR ART in view of GROVER ET AL. (6,055,148).

Art Unit: 2826

The admitted prior art discloses all limitations of claims 10 and 11 except that said second chip is set on top of and is fixed to said first chip, and that said second chip comprises a substrate fixed to said low-voltage region by means of an adhesive layer. Note figures 1 and 2 and pages 1-5 of the instant application

However, Grover et al. discloses an integrated power device comprising a first chip 101 having a low-voltage region 24a and a second chip 102 having a substrate 28, wherein said second chip 102 is set on top of said first chip 101 and said substrate 28 is fixed to said low-voltage region 24a by means of an adhesive layer 110. Note figures 4 and 5 of Grover et al. Therefore, it would have been obvious to a person having skill in the art to augment the admitted prior art's integrated power device by placing the second chip on top of the first chip and fixing the substrate of the second chip to the low-voltage region of the first chip, such as taught by Grover et al. in order to compactly arrange the chips to thus provide a compact, easily protected package.

Allowable Subject Matter

8. Claims 15-17 and 19 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as an integrated power device comprising a power circuit, component, or device comprising a first high-voltage region, a low-voltage region, first and second unidirectional elements connected together between the first high-voltage region and the low-voltage region to define a common intermediate node, a biasing circuit

Art Unit: 2826

connected between the common intermediate node and a second high-voltage region, the biasing circuit comprising a contact pad electrically connected to the common intermediate node, an electrical contact region formed on the second high-voltage region, an electrical connection line having a first end connected to the contact pad and a second end connected to the electrical contact region, an edge structure formed in the power circuit and comprising an equipotential annular region surrounding the power circuit, the contact pad of the biasing circuit being set on top of the equipotential annular region, and a control circuit that includes the second high-voltage region. The just-recited limitations are common to all of claims 14-19.

A. Claims 14 and 18 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112 set forth in this Office action.

B. Claims 2-5 and 12 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 703-308-0980. The examiner can normally be reached on Mon-Thu 8-6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to


Art Unit: 2826

Thomas L Dickey whose telephone number is 703-308-0980. The examiner can normally be reached on Mon-Thu 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TLD
03/2003


Minh Loan Tran
Primary Examiner